Curriculum Vitae

Hans de Vries

Address: Arnhemse straat 94
2587 SW Den Haag
Netherlands
phone: +31-6–38335590
email: hdv@chip-architect.com
date/birth: Aug 13th 1957
online resume information:
http://www.chip-architect.com/mywork.html

Employment History

1998-2007: GenTera, San Mateo, CA , USA
1991-1997: Arcobel Graphics. BV 's-Hertogenbosch
1988-1990: Dataflow Technology Nederland, Den Haag

Well known reputation as Lead Architect for IC / processor-design:

Major Projects: (click on links for more info)

1988	Fifth Generation Computer.	(Custom designed hardware)
1989	High end Graphics Workstation [+]	(Custom designed hardware)
1994	Single chip graphics processor [+]	(ASIC- design)
1999	2nd gen. 3D graphics processor	(ASIC-design)
2005	3D Medical Imaging processor [+]	(ASIC-design)
2008	Author of a post Graduate Physics textbook	(Rel. Quantum Field Theory)

Articles in the professional press on various projects:

- Cover story/special issue: Grafische Superprocessor van Nederlandse bodem
- Article in elektronica: Dataflow wordt marktrijp: Grafische mini super werkt parallel.

Other Professional Activities:

- Well known web-site http://www.chip-architect.com
- Detailed reversed engineering of High End Microprocessors which are used in advanced university courses: eg: Understanding the detailed architecture of AMD's 64 bit core
- Ray tracing projects for highly realistic imaging. eg: image1, image2, image3
- Science Advisor on Physics since 2005 on the webs largest Science Forums site.

Career Timeline:

1998-2007: Lead Architcet at GenTera Inc.. (TeraRecon) (San Mateo, CA)
(GenTera is a Silicon Valley start-up which bought Arcobel Graphics in 1997). I had the Lead Architect responsibility for the development of the MT2 and MT3 single chip graphics processors with many architectural extensions for 3D medical reconstruction, 3D medical/ industrial/ geological volume rendering. 3D ultrasound processing, 3D perspective graphics pipelines, Digital signal and image processing. Video encoding/ decoding, motion detection, radar and sonar processing, et-cetera.

1991-1997: Lead Architect at Arcobel Graphics (The Netherlands)
Arcobel Graphics is a merger of Dataflow technology and Arcobel. The Imagine Graphics processor designed by me was the fastest single chip 3D graphics and image processor by the time it became available. The HISC design principle developed allowed high level RISC processing as well as highly parallel stream processing. Derivatives of the Imagine processor are used world wide for medical and industrial graphics and image processing.

1988-1990: Lead Architect at Dataflow Technology. (The Netherlands)
Dataflow Technology was a management buy-out of PHILIPS and designed a high end, fifth generation parallel computer. The funding came from private investors and the Dutch government. The latter rewarded our project as most promising over competing projects of PHILIPS and the SHELL laboratories, which ended 2nd and 3rd respectively. The Dataflow computer consisted out of local clusters containing 32 dataflow processors each. Local processors where connected via a shared memory bus as well as Banyan token switching network. The world's first C compiler with complete dataflow analysis was developed. It was able to distribute a single C program over multiple parallel processors (Arthur Veen). The Dataflow computer had an High End Graphics Subsystem designed by me consisting out of more then 2000 Integrated Circuits including 16 parallel processors configured for graphics processing. It had video input and output (NTSC, PAL, SECAM) It was able to do image processing an 3D rendering of live video input.

1985-1987: Hardware/ Software design at PHILIPS. The Hague, The Netherlands
Digital Audio studio encoder for D2MAC (European HDTV predecessor) based on a parallel processor based on a 16 dataflow digital signal processor system which I designed. Operating system port for the PHILIPS Image data bank used in the Interactive, Pay per view TV cable system in South Limburg, Work on a multi display information system for the Rotterdam harbor freight shipping bourse (worlds largest) et-cetera.

1984: Free-lance software development for Bitronics, Rijswijk The Netherlands
Database server implementation for Viewdata (Viewdata is an Internet Predecessor)

1982-1984: Free-lance hardware / software development for DAI. Brussels, Belgium
DAI was an INTEL spin-off founded by former Intel employees under the technical leadership of David Lockey, A co-designer of the Intel 8080 micro processor. DAI designed industrial systems and personal computers. The color graphics capabilities of the DAI PC where even better as the Apple II Among the work I did was Graphics hardware design for a follow up model. a software port of Internet predecessor Viewdata network including text editor and graphics editor, down loadable software. Disk drive operating system software etc.

1981-1982: Digital Signal Processing hardware designer at the LEOK laboratories.
Algorithm/hardware design for a NATO project on a Digital Phase Array Sonar system for the automatic detection of location and type of vessels and sub-marines. This project was classified in the category of "NATO Cosmic Top Secret" I was invited to his project because of my theoretical work on Digital Signal Processing during my Final Thesis.

1986 : **ESPRIT advanced course on Future Parallel Computers, Pisa (PostDoc course)**
1977-1981: Electrical Engineering degree from H.T.S. Wegastraat Den Haag

Hands on design experience:

I have designed the following:

- Parallel fifth generation computer with:
  32 Dataflow digital signal processors.
  Global shared memory bus systems and
  Global asynchronous Banyan interconnect networks.
- High end Graphics boards comprising:
  Custom parallel systolic array graphics processors.
  Video I/O processing hardware. (NTSC, PAL,SECAM)
- A Single chip Graphics and Image processor.
- A 3D graphics processor with:
- Open GL compatible perspective 3D rendering pipelines,
  with 3D perspective volume rendering extensions and additions
  for the back-projection of 3D X-ray data (medical / industrial)
- Live video processing capabilities.
- Hardware memory management for 1D, 2D and 3D data.
- Pipelined full precision IEEE floating point Adders and Multipliers.
- Pipelined full precision IEEE floating point hardware
  with single cycle throughput for reciprocal, square root, sine,
  exponent, logarithmic , cosine, arcsine, arccosine functions
- Video Encoding Motion estimation hardware.
- Variable Length Decoding hardware.
- Video Timing generators with multi-board timing synchronization
- Intelligent Very high quality perspective (medical) volume rendering
  pipeline with programmable body tissue awareness.
- Digital video standard IO circuits.
- Digital audio standard IO circuits.
- Serial and parallel standard interfaces.
- Phase Array Sonar Digital Signal Processing hardware.
- DDR Memory interfaces with intelligent timing adjustment circuits.
- On chip data and instruction cache systems.
- VME bus boards.
- VESA bus boards.
- PCI bus boards.

Kind regards, Hans de Vries,

http://www.chip-architect.com/
http://www.physics-quest.org/